

05-7: 4 x 1N4001

7.2 Contents of decode ROM's

I/O \$A0000.
 FF FF FF FF FF FF FF FF FD EF DF CF FF FF FF FF
 FE FB F7 EF FF CF FF CF FF FF FF FF CF FF
 \$S1EE1. N2 I O/1
 tristate or open
 collector

V \$A0000.
 FD FC FF FF FF FF FF FF FF FF FD FD FD FD FF
 FF FF FF FF FF FF FF FF CF FF FF FF FF FD
 \$S1FD1. N2V/2H
 tristate

OP: \$A0000.
 01 00 03 03 03 03 03 03 03 02 03 01 01 01 03
 03 03 03 03 02 03 03 03 03 03 03 03 03 03 01
 \$S0051. N2V/2L
 tristate

MD \$A0000.
 FE FD FB FB F7 F7 FF FF FF FF FF FF FF FF FF
 FF FF FF FF FF EF EF DF DF EF EF 7F 7F 7F 7F
 \$S1CE5. N2MD/3
 open collector
 (binary listing in text)

DB \$A0000.
 F C F C F E F D F E D F C E D D
 F C F C F E F D F E D F D E D D
 F C F C F E F D F E D F C E D D
 F C F C F E F D F E D F C E D D
 F C F C F E F D F E C F C E D D
 F C F C F E F D F E C F C E D D
 F C F C F E F D F E C F C E D D
 F C F C F E F D F E C F C E D D

\$A0000.
 E C E C E E E E E E 9 E C E C C
 E C E C E E E E E E 9 E 9 E C C
 E C E C E E E E E E 9 E C E C C
 E C E C E E E E E E 9 E C E C C
 E C E C E E E E E E C E C E E E
 E C E C E E E E E E C E C E E E
 E C E C E E E E E E C E C E E E
 \$S007C.

N2DB/3H
 tristate
 ('H' version leaves
 unused output bits
 high)

OP: \$A0000.
 7 4 7 4 7 6 7 5 7 6 5 7 4 6 5 5
 7 4 7 4 7 6 7 5 7 6 5 7 5 6 5 5
 7 4 7 4 7 6 7 5 7 6 5 7 4 6 5 5
 7 4 7 4 7 6 7 5 7 6 5 7 4 6 5 5
 7 4 7 4 7 6 7 5 7 6 4 7 5 6 5 5
 7 4 7 4 7 6 7 5 7 6 4 7 4 6 5 5
 7 4 7 4 7 6 7 5 7 6 4 7 4 6 5 5

\$A0000.
 6 4 6 4 6 6 6 6 6 6 1 6 4 6 4 4
 6 4 6 4 6 6 6 6 6 6 1 6 1 6 4 4
 6 4 6 4 6 6 6 6 6 6 1 6 4 6 4 4
 6 4 6 4 6 6 6 6 6 6 1 6 4 6 4 4
 6 4 6 4 6 6 6 6 6 6 4 6 4 6 6 6
 6 4 6 4 6 6 6 6 6 6 4 6 1 6 6 6
 6 4 6 4 6 6 6 6 6 6 4 6 4 6 6 6
 6 4 6 4 6 6 6 6 6 6 4 6 4 6 6 6
 \$S007C.

N2DB/3L
 tristate
 ('L' version leaves
 unused output bits
 low)

7.3 Relationship between N2MD PROM and link pins

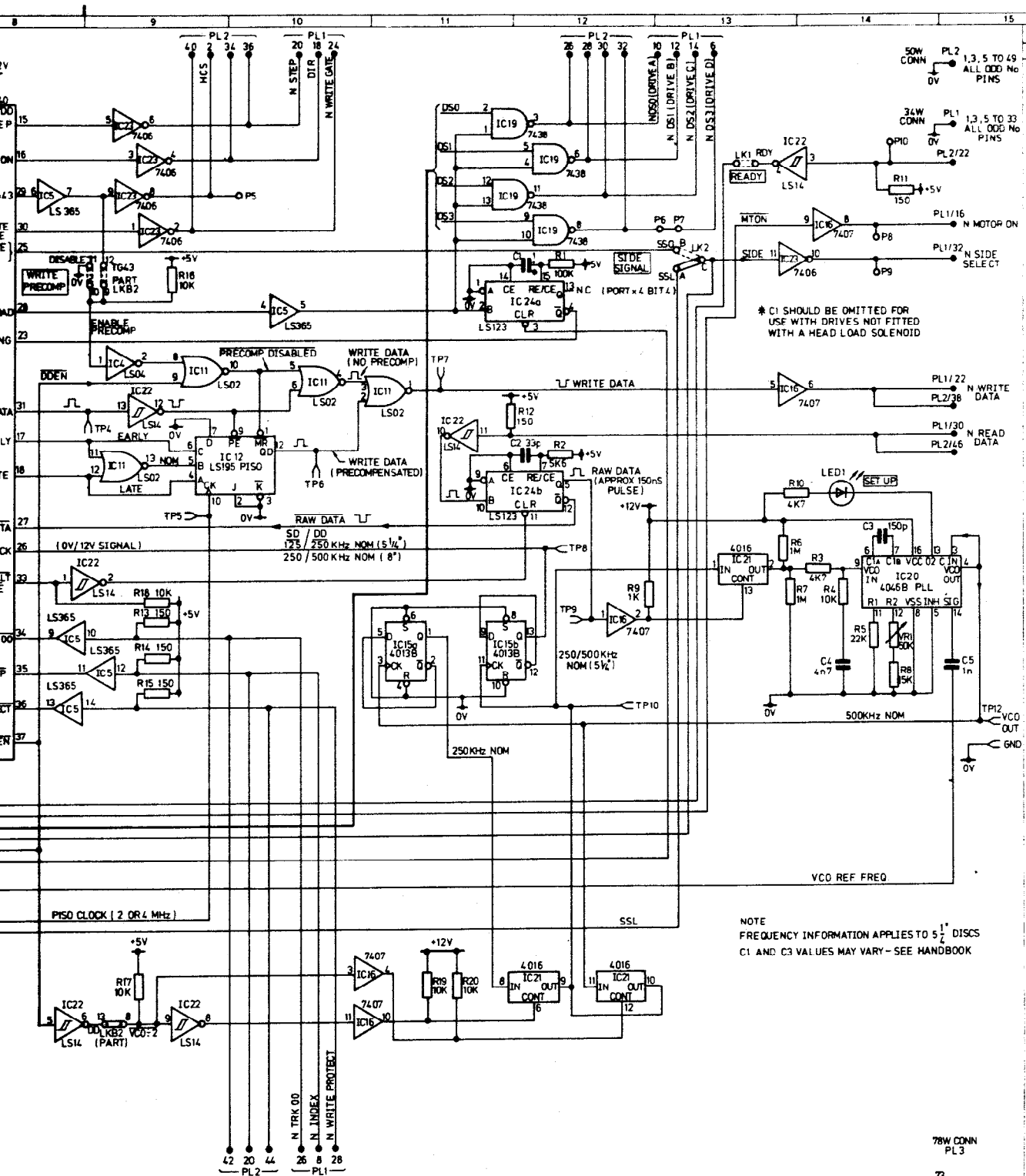
It can be seen from circuit diagrams 3 and 4, that all on board memory (ICs 35;42, 48 and 50) is connected to address lines A0 to A9 which corresponds to 0000 - 03FFH or 1R of addresses. Additionally the MONITOR ROM is connected to A0 to A10 and the BASIC ROM to A0 to A12. The memory devices are enabled one at a time by means of a chip select or chip enable input, CS/CE (active low) which permits memory to be addressed at locations other than 0000H - 07FFH. The chip select function is performed by the N2MD PROM (IC47) in conjunction with the 16pin header plug (LKS1), IC6, IC46, IC69 and switches LSW1/7 and 8.

The MD PROM has 5 inputs (plus active low chip select) which are decoded by internal program, into 32 eight bit patterns, one for each combination of the input. The eight output lines are connected to one side of the 16 pin header. The outputs available from the N2MD PROM are as follows:-

N2MD PROM		OUT-PUT BIT PATTERN											NORMAL USE		
INPUT		D7	D6	D5	D4	D3	D2	D1	D0						
A15	A14	A13	A12	A11	(XXXXX DECODE)										
0000H	- 0	0	0	0	0	(0 Low Half)	1	1	1	1	1	1	1	0	MROM (2K MONITOR ROM)
07FFH	- 0	0	0	0	0		1	1	1	1	1	1	1	0	
0800H	- 0	0	0	0	1		1	1	1	1	1	1	0	1	WRAM (2K WORKSPACE RAM)
0FFFH	- 0	0	0	0	1		1	1	1	1	1	1	0	1	
(0 High Half)															
1000H	- { 0	0	0	1	0	(1)	1	1	1	1	1	0	1	1	4K USER RAM (BLKA + RAMG1)
1FFFH	- { 0	0	0	1	1		1	1	1	1	1	0	1	1	
2000H	- { 0	0	1	0	0	(2)	1	1	1	1	0	1	1	1	4K USER RAM (BLKB + RAM G2)
2FFFH	- { 0	0	1	0	1		1	1	1	1	0	1	1	1	
		0	0	1	0	(3)	1	1	1	1	1	1	1	1	
		0	0	1	1	(4)	1	1	1	1	1	1	1	1	
		0	1	0	0	(5)	1	1	1	1	1	1	1	1	
		0	1	0	1	(6)	1	1	1	1	1	1	1	1	
		0	1	0	1	(7)	1	1	1	1	1	1	1	1	
		0	1	1	0	(8)	1	1	1	1	1	1	1	1	
		0	1	1	1	(9)	1	1	1	1	1	1	1	1	
		1	0	0	0	(A)	1	1	1	1	1	1	1	1	
		1	0	0	1	(B)	1	1	1	1	1	1	1	1	4K SPARE FOR EPROM
B000H	- 1	0	1	1	0		1	1	1	0	1	1	1	1	
BFFFH	- 1	0	1	1	1	(C)	1	1	0	1	1	1	1	1	4K SPARE FOR EPROM
C000H	- 1	1	0	0	0		1	1	0	1	1	1	1	1	
CFFFH	- 1	1	0	0	1	(D)	1	0	1	1	1	1	1	1	4K SPARE FOR EPROM
D000H	- 1	1	0	1	0		1	0	1	1	1	1	1	1	
DFFFH	- 1	1	0	1	1	(E)	0	1	1	1	1	1	1	1	BROM
E000H	1	1	1	0	0		0	1	1	1	1	1	1	1	
		1	1	1	0	(F)	0	1	1	1	1	1	1	1	8K BASIC ROM
		1	1	1	1		0	1	1	1	1	1	1	1	
FFFFH	1	1	1	1	1		0	1	1	1	1	1	1	1	

PIN NAS ON LKS 1:

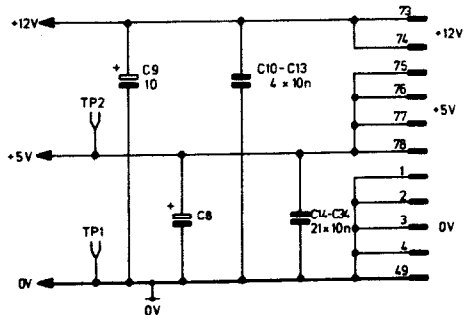
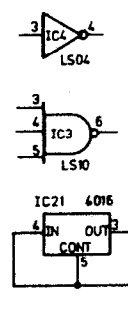
9 10 11 12 13 14 15 16



* C1 SHOULD BE OMITTED FOR USE WITH DRIVES NOT FITTED WITH A HEAD LOAD SOLENOID

NOTE FREQUENCY INFORMATION APPLIES TO 5 1/4 DISCS C1 AND C3 VALUES MAY VARY - SEE HANDBOOK

SARE DEVICES



THIRD ANGLE PROJECTION
DO NOT SCALE
DIMENSIONS IN MM
LIMITS UNLESS OTHERWISE STATED
DIMENSIONS WITH:
NO DECIMAL: ±0.25
ONE DECIMAL: ±0.25
TWO DECIMALS: ±0.10
ANGLES: ±0.5°
FOR INTERPRETATION OF GEOMETRIC TOLERANCE SYMBOLS SEE LUCAS STANDARD No 51-3-5
IF IN DOUBT, ASK

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PARTS LIST No 9929-1148	QTY PER SET	TITLE
ISSUE 1	DATE JAN '82	MATL
CIRCUIT No 9929-1141	FINISH	DRN GCP
ISSUE 1	DATE JAN 82	T.L. DATE JAN '82
ART-WORK No 9929-1142 to 1145	CHKD R. M. G. / S. M. G.	PROJ No
ISSUE	DATE	APPD S. M. G. / S. M. G.

NASCOM	
FLOPPY DISC CONTROLLER	
CIRCUIT DIAGRAM	
ORIGINAL SCALE	JOB No

Lucas
Lucas Logic Limited
Wellton Road
Wedgwood Industrial Estate
Warwick CV34 5PZ
SHEET 1 OF 1
9929-1141

WHEN REFERRING TO THIS DRAWING
 QUOTE LATEST CHANGE SYMBOL

