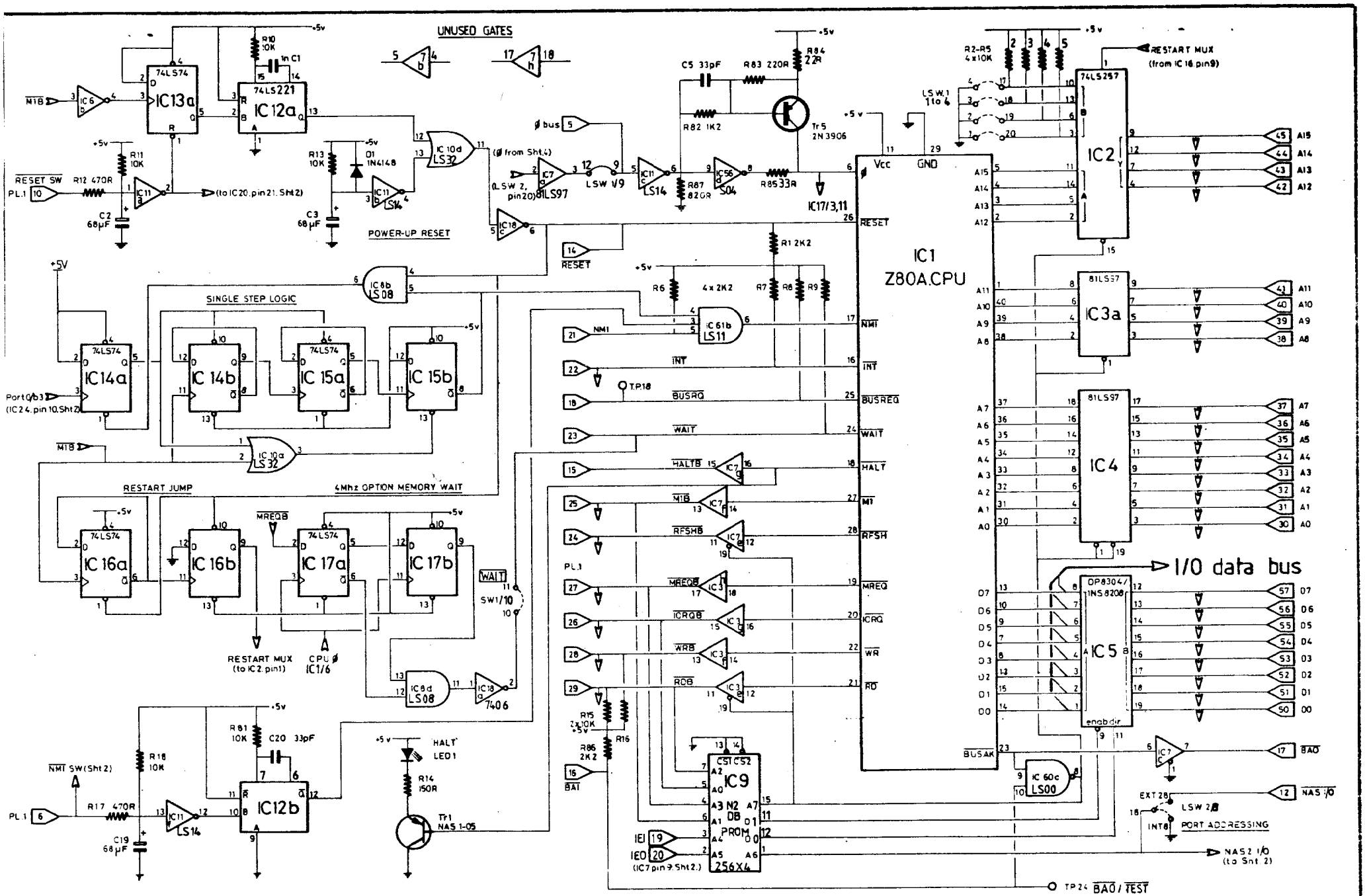
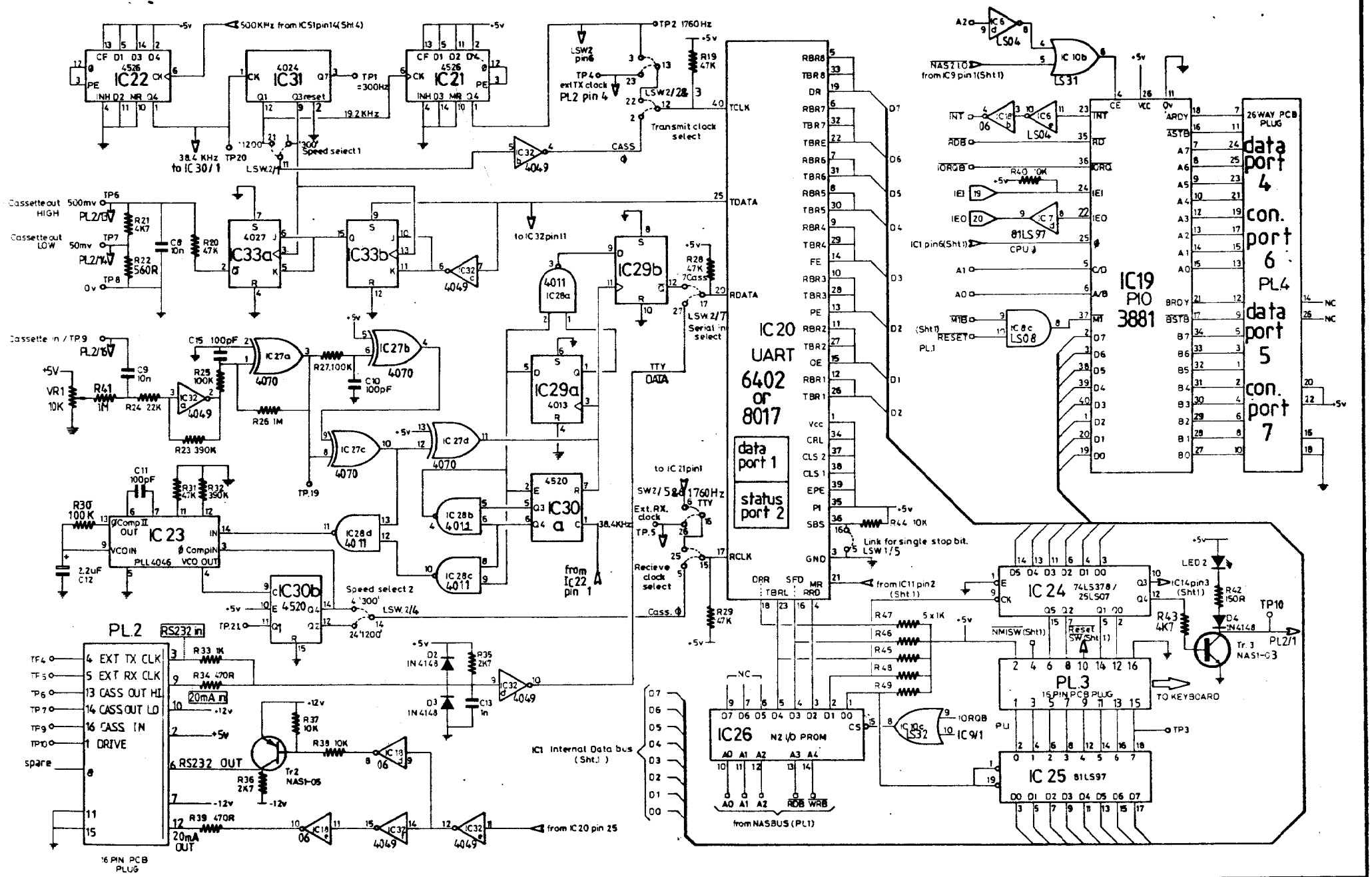
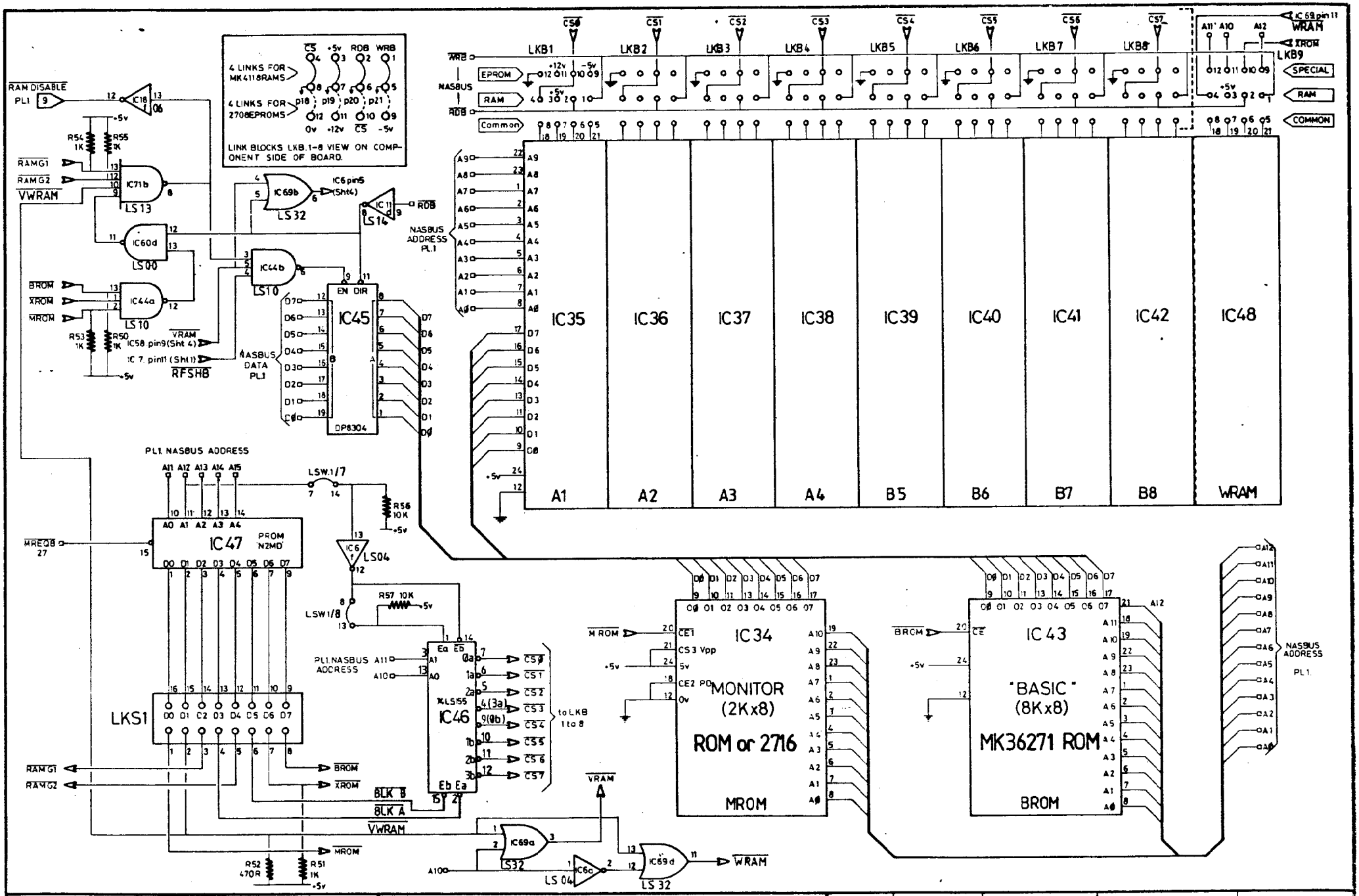


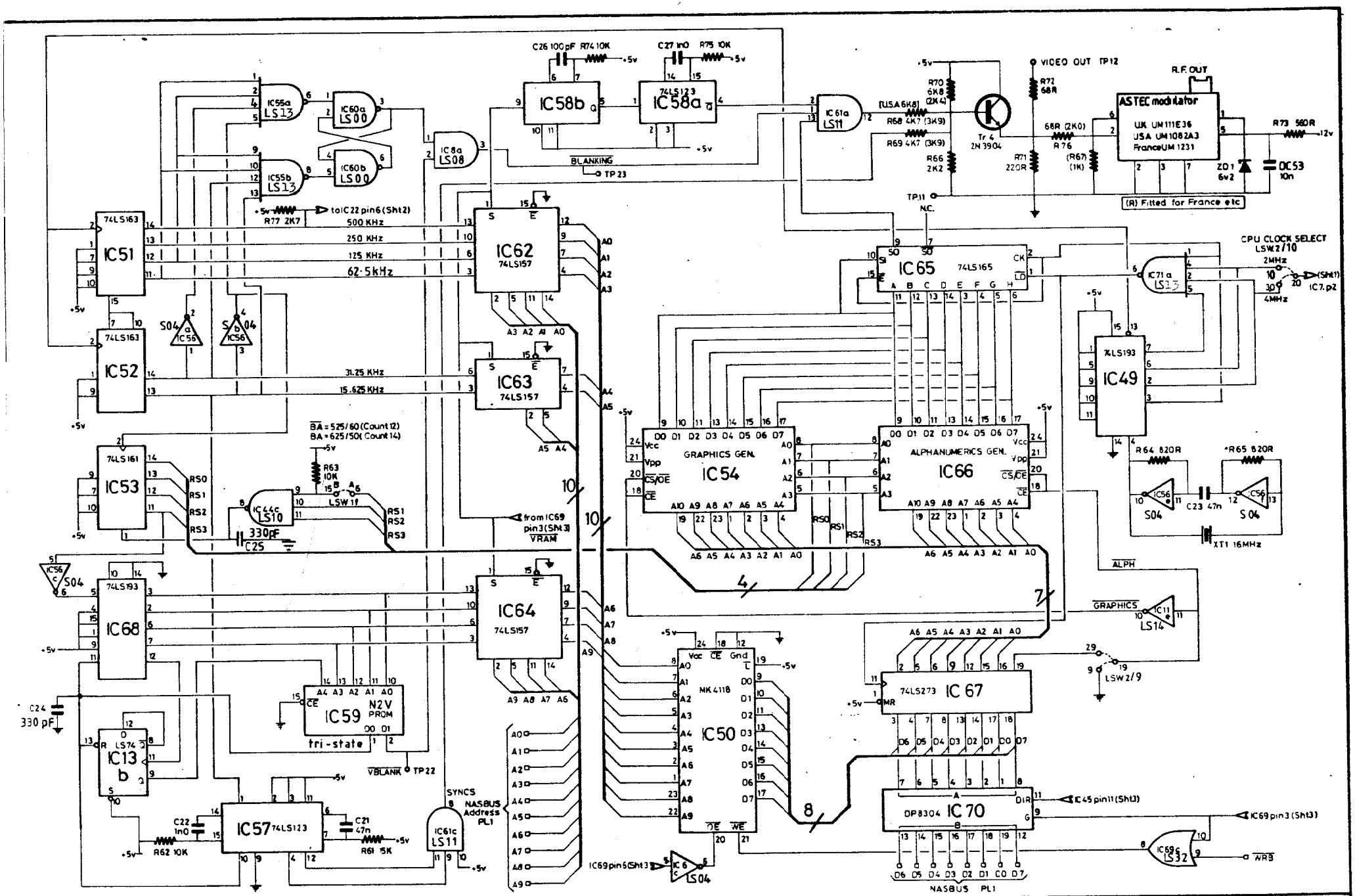
Nascom Microcomputers	NASCOM 2 CPU	Issue 8	Sht 1 of 5	Drawn	Checked	Date 16-6-79
		Revisions :- revision 6/11/1079		Drawing no. 022-401		



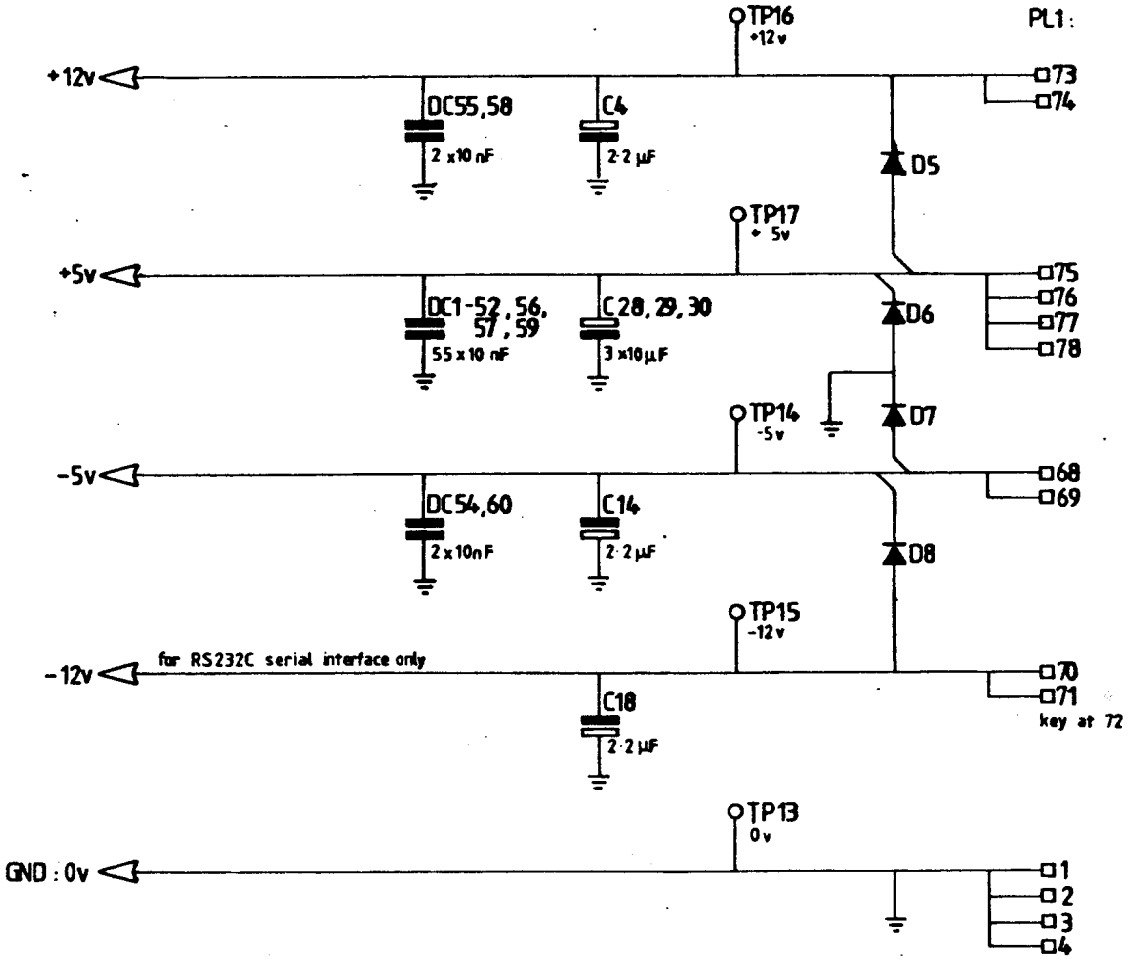
Nascom Microcomputers	NASCOM 2 — Input/Output	Issue 8	Sht 2 of 5	Drawn	Checked	Date 17-6-79
		Revisions			Drawing no	022-402



Nascom Microcomputers	NASCOM 2 Memory	Issue 8	Sht 3 of 5	Drawn	Checked	Date 16-6-79
		Revisions			Drawing no. 022-403



Nascom Microcomputers	NASCOM 2-Video	Issue 8 | Sht 4 of 5 | Drawn	Checked	Date 20-6-79
		Revisions	Drawing no. 022-404	



D5-7: 4 x 1N4001

Nascom Microcomputers	NASCOM 2-Power Distribution	Issue 8	Sht 5 of 5	Drawn	Checked	Date 11·10·79
		Revisions:		Drawing no. 022 - 405	

7.2 Contents of decode ROM's

I/O

```
$A0000,
FF FF FF FF FF FF FF FF FD EF DF 7F FF FF FF FF
FE FB F7 BF FF 7F FF 7F FF FF FF 7F FF FF 7F FF
$S1EE1,
```

N2 I 0/1
tristate or open collector

V

```
$A0000,
FD FC FF FF FF FF FF FF FF 7F FF FD FD FD FD FF
FF FF FF FF FF FF FF FF FF 7F FF FF FF FF FF FD
$S1FD1,
```

N2V/2H
tristate

---

or:

```
$A0000,
01 00 03 03 03 03 03 03 03 03 03 01 01 01 01 03
03 03 03 03 03 03 03 03 03 03 03 03 03 03 03 01
$S0051,
```

N2V/2L
tristate

MD

```
$A0000,
FE FD FB FB F7 F7 FF FF FF FF FF FF FF FF FF FF
FF FF FF FF FF FF EF EF DF DF BF BF 7F 7F 7F 7F
$S1CE5,
```

N2MD/3
open collector
(binary listing in text)

DB

```
$A0000,
F C F C F E F D F E D F C E D D
F C F C F E F D F E D F D E D D
F C F C F E F D F E D F C E D D
F C F C F E F D F E D F C E D D
F C F C F E F D F E C F C E D D
F C F C F E F D F E C F D E D D
F C F C F E F D F E C F C E D D
F C F C F E F D F E C F C E D D

$A0080,
E C E C E E E E E E 9 E C E C C
E C E C E E E E E E 9 E 9 E C C
E C E C E E E E E E 9 E C E C C
E C E C E E E E E E 9 E C E C C
E C E C E E E E E E C E C E E E
E C E C E E E E E E C E 9 E E E
E C E C E E E E E E C E C C E E
E C E C E E E E E E C E C E E E
$S0D7C,
```

N2DB/3H
tristate
('H' version leaves unused output bits high)

---

or:

```
$A0000,
7 4 7 4 7 6 7 5 7 6 5 7 4 6 5 5
7 4 7 4 7 6 7 5 7 6 5 7 5 6 5 5
7 4 7 4 7 6 7 5 7 6 5 7 4 6 5 5
7 4 7 4 7 6 7 5 7 6 5 7 4 6 5 5
7 4 7 4 7 6 7 5 7 6 4 7 4 6 5 5
7 4 7 4 7 6 7 5 7 6 4 7 5 6 5 5
7 4 7 4 7 6 7 5 7 6 4 7 4 6 5 5
7 4 7 4 7 6 7 5 7 6 4 7 4 6 5 5

$A0080,
6 4 6 4 6 6 6 6 6 6 1 6 4 6 4 4
6 4 6 4 6 6 6 6 6 6 1 6 1 6 4 4
6 4 6 4 6 6 6 6 6 6 1 6 4 6 4 4
6 4 6 4 6 6 6 6 6 6 1 6 4 6 4 4
6 4 6 4 6 6 6 6 6 6 4 6 4 6 6 6
6 4 6 4 6 6 6 6 6 6 4 6 1 6 6 6
6 4 6 4 6 6 6 6 6 6 4 6 4 6 6 6
6 4 6 4 6 6 6 6 6 6 4 6 4 6 6 6
$S057C,
```

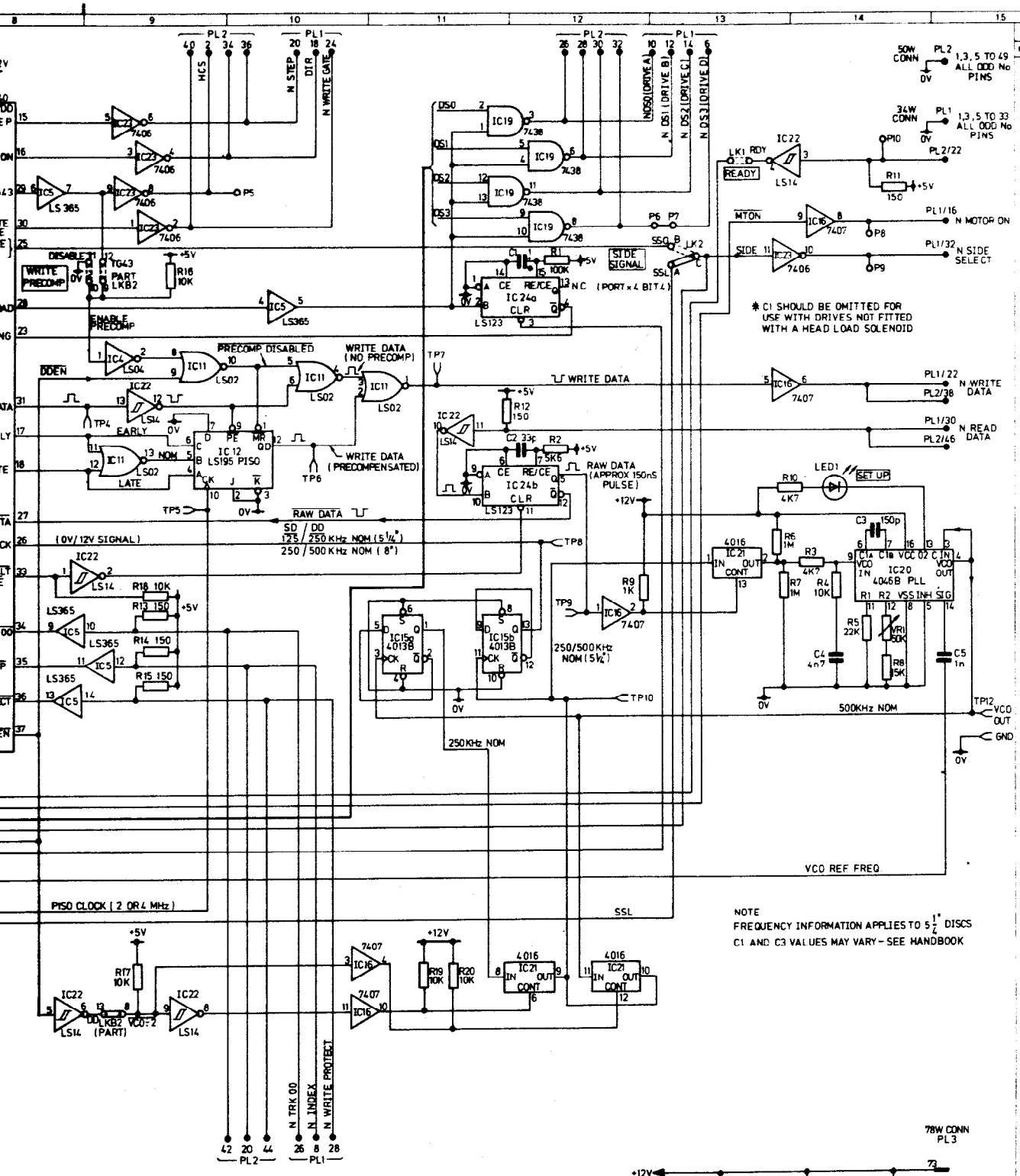
N2DB/3L
tristate
('L' version leaves unused output bits low)

7.3 Relationship between N2MD PROM and link pins

It can be seen from circuit diagrams 3 and 4, that all on board memory (ICs 35;42, 48 and 50) is connected to address lines AØ to A9 which corresponds to ØØØØ - Ø3FFH or 1R of addresses. Additionally the MONITOR ROM is connected to AØ to AlØ and the BASIC ROM to AØ to A12. The memory devices are enabled one at a time by means of a chip select or chip enable input, CS/CE (active low) which permits memory to be addressed at locations other than ØØØØH - Ø7FFH. The chip select function is performed by the N2MD PROM (IC47) in conjunction with the 16pin header plug (LKS1), IC6, IC46,IC69 and switches LSW1/7 and 8.

The MD PROM has 5 inputs (plus active low chip select) which are decoded by internal program, into 32 eight bit patterns, one for each combination of the input. The eight output lines are connected to one side of the 16 pin header. The outputs available from the N2MD PROM are as follows:-

	N2MD PROM INPUT						OUT-PUT BIT PATTERN								
	A15	A14	A13	A12	A11	(XXXXX DECODE)	D7	D6	D5	D4	D3	D2	D1	DØ	NORMAL USE
ØØØØH - Ø7FFH	Ø	Ø	Ø	Ø	Ø	(Ø Low Half)	1	1	1	1	1	1	1	Ø	$\overline{\text{MROM}}$ (2K MONITOR ROM)
Ø8ØØH - ØFFFH	Ø	Ø	Ø	Ø	1		1	1	1	1	1	1	Ø	1	$\overline{\text{WRAM}}$ (2K WORKSPACE RAM)
						(Ø High Half)									
1ØØØH - 1FFFH	Ø	Ø	Ø	1	Ø	(1)	1	1	1	1	1	Ø	1	1	4K USER RAM (BLKA + RAMG1)
	Ø	Ø	Ø	1	1		1	1	1	1	1	Ø	1	1	
2ØØØH - 2FFFH	Ø	Ø	1	Ø	Ø	(2)	1	1	1	1	Ø	1	1	1	4K USER RAM (BLKB + RAM G2)
	Ø	Ø	1	Ø	1		1	1	1	1	Ø	1	1	1	
	Ø	Ø	1	1	Ø	(3)	1	1	1	1	1	1	1	1	
	Ø	Ø	1	1	1		1	1	1	1	1	1	1	1	
	Ø	1	Ø	Ø	Ø	(4)	1	1	1	1	1	1	1	1	
	Ø	1	Ø	Ø	1		1	1	1	1	1	1	1	1	
	Ø	1	Ø	1	Ø	(5)	1	1	1	1	1	1	1	1	
	Ø	1	Ø	1	1		1	1	1	1	1	1	1	1	
	Ø	1	1	Ø	Ø	(6)	1	1	1	1	1	1	1	1	
	Ø	1	1	Ø	1		1	1	1	1	1	1	1	1	
	Ø	1	1	1	Ø	(7)	1	1	1	1	1	1	1	1	
	Ø	1	1	1	1		1	1	1	1	1	1	1	1	
	1	Ø	Ø	Ø	Ø	(8)	1	1	1	1	1	1	1	1	
	1	Ø	Ø	Ø	1		1	1	1	1	1	1	1	1	
	1	Ø	Ø	1	Ø	(9)	1	1	1	1	1	1	1	1	
	1	Ø	Ø	1	1		1	1	1	1	1	1	1	1	
	1	Ø	1	Ø	Ø	(A)	1	1	1	1	1	1	1	1	
	1	Ø	1	Ø	1		1	1	1	1	1	1	1	1	
BØØØH - BFFFH	1	Ø	1	1	Ø	(B)	1	1	1	Ø	1	1	1	1	4K SPARE FOR EPROM
	1	Ø	1	1	1		1	1	1	Ø	1	1	1	1	
CØØØH - CFFFH	1	1	Ø	Ø	Ø	(C)	1	1	Ø	1	1	1	1	1	4K SPARE FOR EPROM
	1	1	Ø	Ø	1		1	1	Ø	1	1	1	1	1	
DØØØH - DFFFH	1	1	Ø	1	Ø	(D)	1	Ø	1	1	1	1	1	1	4K SPARE FOR EPROM
	1	1	Ø	1	1		1	Ø	1	1	1	1	1	1	
EØØØH - FFFFH	1	1	1	Ø	Ø	(E)	Ø	1	1	1	1	1	1	1	$\overline{\text{BROM}}$
	1	1	1	Ø	1	(F)	Ø	1	1	1	1	1	1	1	8K BASIC ROM
	1	1	1	1	Ø		Ø	1	1	1	1	1	1	1	
	1	1	1	1	1		Ø	1	1	1	1	1	1	1	
						PIN NAS ON LKS 1:	9	10	11	12	13	14	15	16	



NOTE
FREQUENCY INFORMATION APPLIES TO 5¼" DISCS
C1 AND C3 VALUES MAY VARY - SEE HANDBOOK

SPARE DEVICES

THIRD ANGLE PROJECTION

DO NOT SCALE

DIMENSIONS IN MM

LIMITS UNLESS OTHERWISE STATED
DIMENSIONS WITHIN
NO DECIMAL ±0.2 ±0.6
ONE DECIMAL ±0.2 ±0.2
TWO DECIMALS ±0.02 ±0.05
ANGLES ± 0.5°

FOR INTERPRETATION OF GEOMETRICAL TOLERANCE SYMBOLS SEE LUCAS STANDARD No 51-3-5

IF IN DOUBT, ASK

CHANGES	DATE ISS
FIRST DRAWN	JAN 82

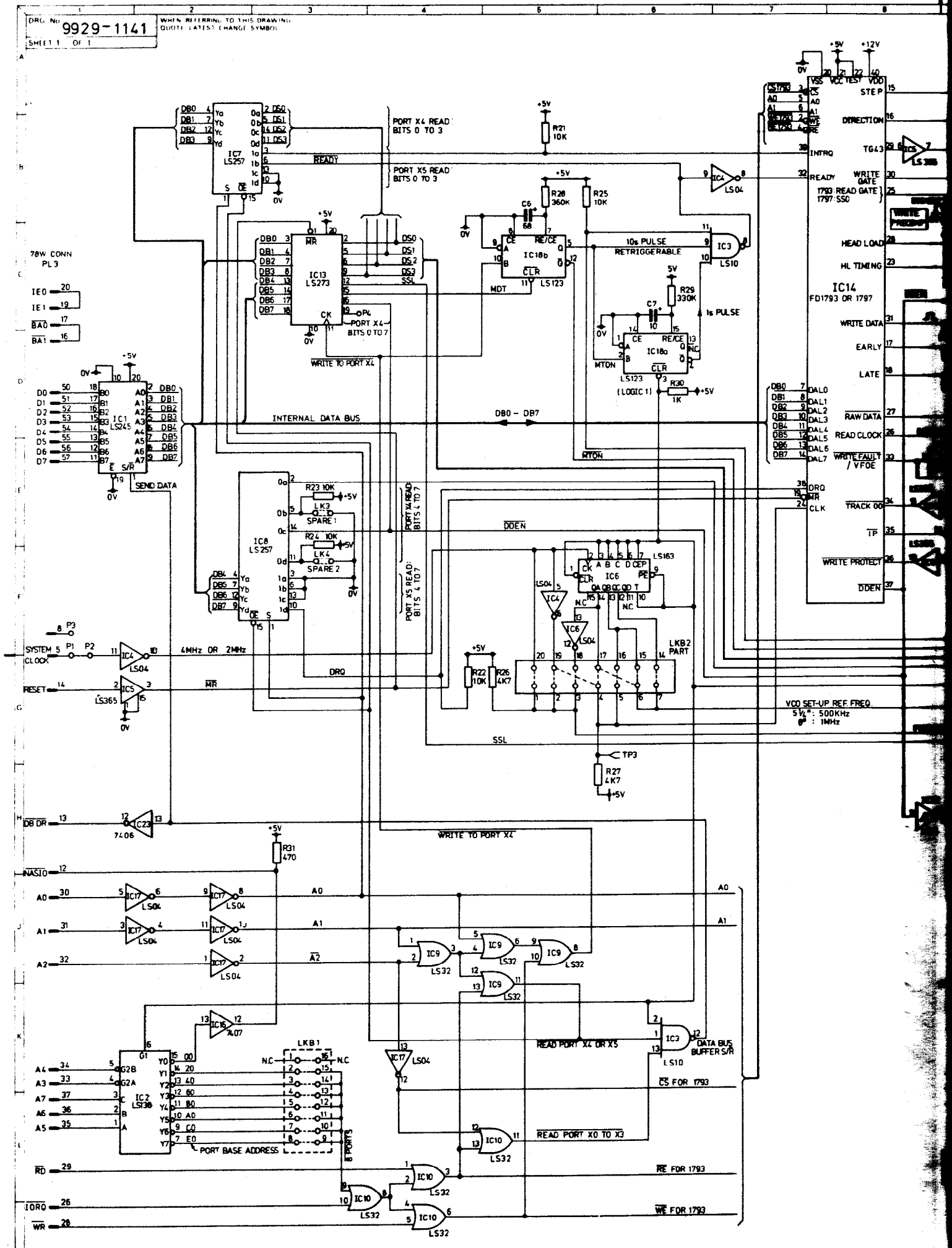
PARTS LIST No 9929-1148		QTY PER SET	
ISSUE 1	DATE JAN '82	MAT'L	
CIRCUIT No 9929-1141		FINISH	
ISSUE 1	DATE JAN '82	DR'N GCP T.L.	DATE JAN'82
ART-WORK No 9929-1142 to 1145		CHK'D	
ISSUE	DATE	APP'D	

TITLE NASCOM
FLOPPY DISC CONTROLLER
CIRCUIT DIAGRAM

PROJ No | JOB No
ORIGINAL SCALE

Lucas
Lucas Logic Limited
Welton Road
Wedgnock Industrial Estate
Warwick CV34 5PZ

SHEET 1 OF 1
DRG No 9929-1141


DRG. No 9929-1141
SHEET 1 OF 1
WHEN REFERRING TO THIS DRAWING QUOTE LATEST CHANGE SYMBOL
IC7 LS257
PORT X4 READ BITS 0 TO 3
PORT X5 READ BITS 0 TO 3
READY
R21 10K
R28 360K
R25 10K
C6 68
IC18b
10s PULSE RETRIGGERABLE
IC3 LS10
IC4 LS04
IC13 LS273
WRITE TO PORT X4
MDT
IC18a
LS123
C7
1s PULSE
R29 330K
MTON
(LOGIC 1)
R30 1K
78W CONN PL3
IC1 LS245
INTERNAL DATA BUS
DB0 – DB7
SEND DATA
IC8 LS257
R23 10K
LK3 SPARE 1
R24 10K
LK4 SPARE 2
PORT X4 READ BITS 4 TO 7
PORT X5 READ BITS 4 TO 7
DDEN
LS163
IC6
LKB2 PART
SYSTEM CLOCK
4MHz OR 2MHz
RESET
DRQ
MR
R22 10K
R26 4K7
VCO SET-UP REF. FREQ.
5¼": 500KHz
8": 1MHz
SSL
TP3
R27 4K7
IC14 FD1793 OR 1797
STEP
DIRECTION
INTRQ
WRITE GATE
1793: READ GATE
1797: SSO
HEAD LOAD
HL TIMING
WRITE DATA
EARLY
LATE
RAW DATA
READ CLOCK
WRITE FAULT / VFOE
TRACK 00
TP
WRITE PROTECT
DDEN
DB DR
7406
IC23
WRITE TO PORT X4
R31 470
INASIO
A0
A1
A2
IC17 LS04
IC9 LS32
IC15 7407
IC2 LS138
LKB1
PORT BASE ADDRESS
8 PORTS
READ PORT X4 OR X5
DATA BUS BUFFER S/R
CS FOR 1793
READ PORT X0 TO X3
RE FOR 1793
WE FOR 1793
RD
IORQ
WR