nascom

Nascom Microcomputer DOCUMENTATION

HARDWARE MANUAL

FOR THE

ADVANCED VIDEO CARD
(AVC MODEL B)

Issue 2.1.

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Lucas Logic

AVC (MODEL B)

HARDWARE MANUAL

VERSION 2.1

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CHAPTER 1

"WHAT IS THE AVC"

"AVC" stands for ADVANCED VIDEO CONTROLLER, and is a NASCOM peripheral card providing high quality colour graphics and text for microcomputers.

"what's in this manual"

This manual describes the operation of the hardware of the AVC, and how it is interfaced to the outside world. It is VITAL that this manual is read completely before any attempt is made to use the AVC.

Depending on the the system the following manuals should be consulted;

COLOUR GRAPHICS SOFTWARE MANUAL

AVC TERMINAL MANUAL

other SYSTEM MANUALS

CHAPTER 2

"operation of the AVC"

This manual refers to AVC MODEL B ONLY

This chapter requires reference to the AVC circuit diagrams: see APPENDIX 1.

The AVC contains three video memory planes which are normally assigned to the three primary colours RED,GREEN and BLUE. Each PIXEL (picture element) on the screen is allocated a bit in the R,G and B planes thus allowing eight different codes per pixel. The pixels are arranged as a raster of 512 by 256, which is 64 bytes by 256 bytes, thus a total of 64*256=16384 or 16Kbytes per colour plane.

Of the 512 possible pixels available on a horizontal line only 392 are available using the standard AVC configuration, this is because the remaining pixels are blanked to provide margins at the side of the display and to allow time for the display to retrace.

The AVC is configured as three 16K byte memory planes (R,G,B) of which only about 76% are used for display purposes, these planes are shown on sheet 2 of the circuit diagram.
Each of the three planes consists of eight 16k by 1 bit memory chips (type 4116-3), the planes use ICs 1 to 24.
The rest of the circuitry shown on sheet 2 shows the read data bus buffer/latches (ICs 26,28,30),the write data bus buffer (IC 25),resisters to reduce ringing (RP1,RP2,R21-R25) and finally the /CAS selection circuit. The final section acts as the decode circuit for the colour planes.

Each of the memory chips uses multiplexing of it's address lines to save pin space,the /RAS strobes the ROW ADDRESS and the /CAS stobes the COLUMN ADDRESS.

Now refer to sheet 1 for the remaining description.

The heart of the AVC is the timing circuitry and is formed by the crystal and ICs 43 & 49. The standard crystal frequency is 16.25 MHz, this rather strange frequency is used so that the horizontal sync frequency is exactly 64 uSEC, this is required for PAL colour. Note it is possible to change the frequency of this crystal to increase the resolution of the AVC, however if taken too high then the /RAS and /CAS delays may have to be changed, this normally occurs between 18 and 20 MHz. The /RAS,/CAS generation circuitry is formed by ICs around position 6J on the circuit.

Because the video memory is formed from dynamic ram it requires a read,write or refresh to be performed on each of it's row addresses every 2 MSEC to maintain valid data, this function is achieved by the CRTC (cathode ray tube controller) when it reads data from the memory to display on the screen. This requires that

the CRTC be initialised before the AVC memory can be used otherwise data will be corrupted. The CRTC used is a 6845 type and is used to generate all the video timing required by the display device, it also generates the signals which scan the video memory to read the data required to display. The 6845 type CTRC is normally used for alpha-numeric display systems but can be used for graphics displays by introducing the normal character generator ROW address lines into the memory address lines, this technique allows the CRTC to access up to 16K bytes of memory.

The CRTC accesses the video memory once every microsecond, fetching three bytes (R,G,B), this is required to make data available for display purposes and to provide refresh for the dynamic ram. The processor requires to be able to both read from and write to the video memory, giving the processor the overide option produces the screen flash that is visible on the NASCOM 2. Using only the blanking period reduces the read/write speed, so to provide fast response the processor access is time multiplexed between the CRTC access. This multiplexing is achieved by the circuitry at G4 and G6 on sheet 1, this circuitry also provides the /RAS,/CAS multiplexing.

The AVC colour planes are accessed using page mode, this can be thought of as a deck of four cards ;

the normal processor memory

the red plane

the green plane

the blue plane

When any of the AVC planes are paged in, the normal processor memory is paged out thus protecting any program/data which may be stored there. The AVC planes can be paged in any combination, and as they all start at the same address data can be read/written to multiple planes simultaneously. thus to write a white byte (or pixel) all three planes are paged in providing white, note red,green and blue form white. Although it is possible to write to more than one plane simultaneously, only one plane can be read at one time. The circuitry which prevents this possible bus clash is located B11 on sheet 1.

The start of the AVC planes will be normally set to 8000 HEX, as this is the address that the software expects. The links located near IC61 on the AVC allow the start address to be changed.

NOTE ALL LINKS ON THE AVC ARE SET UP IN THERE STANDARD CONFIGURATION USING PCB TRACKS. THESE HAVE TO BE CUT TO EFFECT ANY CHANGES.

C the common link connection
1 locates the AVC planes at 0000 HEX
2 locates the AVC planes at 4000 HEX
3 locates the AVC planes at 8000 HEX (standard link)
4 locates the AVC planes at C000 HEX

The circuitry located at F5 on sheet 1 controls the processor access.

There are three I/O ports used by the AVC these are normally located at;

PORT B0 HEX CRTC address register
PORT B1 HEX CRTC data register
PORT B2 HEX AVC control register

Ports 0B0H and 0B0H are used to control the CRTC and are used as follows;

Port 0B0H is a "pointer" register, it controls which of the 18 CRTC registers appear at port 0B1H, and is a write only register.

ADDRESS REGISTER VALUE	DATA REGISTER SELECTED
0	HORIZONTAL TOTAL (- 1 count)
1	HORIZONTAL DISPLAYED
2	H. SYNC POSITION
3	H. SYNC WIDTH
4	VERTICAL TOTAL (-1 count)
5	V. TOTAL ADJUST
6	VERTICAL DISPLAYED
7	V. SYNC POSITION
8	INTERLACE MODE
9	MAX SCAN LINE ADDRESS
10	CURSOR START
11	CURSOR END
12	START ADDRESS(H)
13	START ADDRESS(L)
14	CURSOR(H)
15	CURSOR(L)
16	LIGHT PEN(H)
17	LIGHT PEN(L)

The clock frequency (Tc) for the CRTC is 2 MHz, for programming details of the CTRC refer to the MOTOROLA MC6845 data manual. The remaining port is used to control system functions of the AVC it's functions are;

Port ØB2H control port

Bit Ø RED plane page select into memory
Bit 1 GREEN plane page select into memory
Bit 2 BLUE plane page select into memory
Bit 3 DOUBLE DENSITY select
Bit 4 RED video output select
BIT 5 GREEN video output select
Bit 6 BLUE video output select
Bit 7 EXTERNAL video select

All controls functions are active on (high).

The addresses of the three ports can be changed using the link block located near IC 44.

LK1 (CRTC address) is selected by default to be ØBØH
LK2 (CTRC DATA) is selected by default to be ØB1H
LK3 (control) is selected by default to be ØB2H

If an address change is required the break these links and connect to the other address, ports ØB3H to ØB9H are available.

I M P O R T A N T N O T E

NOTE The control port can power up configured to any state, this is the reason that O B2 8Ø has to be used on system power up.

All the resisters marked with a "*" on the circuit diagram are used as open-collector pull-ups, if more than one resister is already present on these lines, then these resisters may be removed.

Link 13 provides the facility of grounding line 49 of the bus if required, it is not grounded by default.

Link 4 provides a NASCOM 2 EXT I/O signal decoded to be the first 128 I/O addresses, if this is not required then break this link. The light pen strobe input of the CTRC is normally grounded by link 12. If a light pen is required then changing this link will provide a light pen input on the LIGHT PEN test point. Note care must be taken that this line is not asserted on power up or with a CRTC RESET otherwise the CTRC will go into it's test mode, refer to the MOTOROLA MC6845 data manual. It should be noted that the CTRC does not contain full specification bus drivers and hence on very large systems there may be some problems with bus driving when using the light pen input.

A hardware cursor facility is povided on the CURSOR test point and if required can be linked to the required output circuit, the usual way is XOR the cursor and the video.

Link 6 defines whether the CRTC will be write protected (to allow multiple AVCs) this is normally in the NON write protect position.

Link 5 normally grounds the CRTC RESET line, if the AVC is required to be syncronised to an external source then this link should be broken and the external sync connected to the /RES connector (test point or I/O connector), note to achieve correct syncronisation the CRTC should be initialised to have a frame time in excess of that of the external signal. The scan rate cannot be syncronised unless the two signals are locked using the master timing generator.

The circuitry formed by IC 58 generates a timing signal for the CRTC.

The data out of the three memory planes is routed to the three parallel to serial converters formed by IC 27,29,31. The control signals for the three shift registers are generated by the circuitry at L6 on sheet 1.

The capacitors C13 & C135 control the switch over between bytes when in double density mode.

The capacitor C136 controls the switch over between bytes when in the single density mode.

NOTE If there are problems with pixel flash then the value of these capacitors should be changed slightly.

Hardware blanking is generated by the capacitor C14 (at D5), if hardware scroll (using 20 lines of text, with 12 scan lines per character row) is required then this circuit should be disabled, it is required for PAL TV generation only.

The outputs from the shift registers form the normal R,G,B serial outputs at a resolution of 392 by 256. To select double density the RED and GREEN planes are connected together in a serial fashion and the shift register clock rates doubled to provide a resolution of 784 by 256. This arrangement leaves the BLUE plane unused and can still be displayed as normal. The serial input and output of the BLUE shift register is available on test pins, enabling the connection of 2 AVCs to provide 785 by 256 with 8 colour graphics. When using 2 AVCs the video outputs will have to be resyncronised using latches. Links 14 and 15 normally only connect the BLUE shift register to the single density signals, changing the links provides the double density signals when the double density control bit is activated.

The outputs from the three planes are routed through selection circuitry formed by IC 51 and IC 64, this introduces blanking and provides selection of each individual plane and also a external video source.

The final output is available at test pins and at the I/O connector in TTL form, a composite video signal formed from the "OR" of the three planes, a "GREY" scale and R,G,B 1v pk/pk are available from the coax sockets.

CHAPTER 3

INPUT / OUTPUT TEST PINS

AVC TEST PINS (all levels are TTL)

TEST PIN	FUNCTION
1	/RES :CRTC RESET
2	VSYNC OUT
3	HSYNC OUT (note external syncs are not available at test pins 2 or 3)
4	DISPLAY ENABLE (note this does not include the extra PAL blanking provided by the BLANKing output)
5	EXTERNAL SYNC INPUT (used for nascom /sync)
6	EXTERNAL VIDEO INPUT (used for nascom video)
7	AVC SYNC (this is a tap before the external syncs are added and is normally a copy of the /SYNC signal, it can be used as an external AVC input /SYNC if link 7 is broken)
8	/SYNC OUT
9	/BLANK OUT
10	BLUE OUTPUT
11	GREEN OUTPUT
12	RED OUTPUT
13	BLUE SERIAL OUTPUT
14	BLUE SERIAL INPUT
15	SPARE
16	ZERO VOLTS,GROUND
17	/RAMDIS

All the three I/O connectors have pin 1 marked on the board and are numbered in a zig-zag fashion, the same as for the Nascom 2.

The pinout of I/O connectors are as follows

The AVC external connector PL 1

PIN	TEST PIN	SIGNAL
1	TP12	Red TTL O/P
2	Ground	Ø volts
3	spare	
4	TP8	/sync TTL comp. O/P
5	TP10	Blue TTL O/P
6	TP11	Green TTL O/P
7	TP6	Ext TTL video -
8	TP1	CRTC /RES TTL
9	TP5	Ext TTL /sync -
10	TP7	Ext TTL /sync via link 7
11	Ground	
12	"	
13	"	
14	"	
15	"	
16	"	

The PAL encoder connector PL 2

PIN	SIGNAL
1	Red
2	Green
3	Blue
4	/sync
5	Alternate line sync
6	/alternate line sync
7	Burst gate
8	/burst gate
9	4 MHz clock
10	H sync
11	+5 volts
12	+12 volts
13	Ground Ø volts
14	"
15	"
16	"

The Colour plane selection connector PL 3

PIN	SIGNAL
1	plane C to Green
2	plane B to Green
3	plane A to Blue
4	plane A to Green
5	plane B to Blue
6	plane C to Red
7	spare
8	plane B to Red
9	spare
10	plane A to Red
11	spare
12	spare
13	plane C to blue
14	spare
15	V sync
16	Ground Ø volts
17 to 26	spare

The pin connections of this connector are exactly the same as the Nascom 2 PIO connector. The purpose of this connector is to allow the re-definition of the colours of the three primary planes. A straight (pin for pin) connection is made between this connector (AVC PL 3) and the Nascom 2 parallel connector (NASCOM 2 PL 4).

This connector allows the user to re-define the colours of the planes, this facility is normally linked out so that the colour definition logic is bypassed. There are three bypass links;

LINK 10 controls blue
LINK 9 controls green
LINK 8 controls red

C is the common connection for the links
1 is the bypass connection (standard pcb track)
2 is the re-definition connection

Each primary colour output has software selectable switching connecting it to the three video planes A,B and C. Thus each of the three primary colour outputs (called R,G and B) can be redefined as a combination of the three video planes.
Each channel has three control bits which select the combination of input planes, these can be controlled by switches,external logic or from the Nascom 2 PIO.
If a direct cable is used then the control bits of the colour logic relate to the following PIO lines;

PORT B BIT	0 controls	red video plane to	red output
	1	green	
	2	blue	
	3	red	green
	4	green	
	5	blue	
	6	red	blue
	7	green	
PORT A BIT	0	blue	

1 is an output (from the AVC) and is the V sync signal. This can be used to syncronise the colour changes to the blanking period.

CHAPTER 4

EXTERNAL CONNECTIONS TO THE AVC

EXTERNAL VIDEO from the NASCOM 2

Connect the EXTERNAL VIDEO input of the AVC (TP6) to pin 12 of IC 61 (Nascom 2) and connect the EXTERNAL /SYNC input of the AVC (TP5) to pin 8 of IC 61 (Nascom 2).

COLOUR TTL MONITOR connection

RED	to	TP12	
GREEN	to	TP11	
BLUE	to	TP10	NB. or to the I/O connector
/SYNC	to	TP8	
GROUND	to	TP16	

Colour monitor. (Compositive PAL input) use the PAL encoder card.
Note. This also applies to video recorders even if they have TTL R,G,B inputs.
The PAL encoder produces a lower bandwith signal.

Colour monitor. (1 volt pk/pk seperate RGB with compositive /sync on green).

RED	to	Rcom coax socket
GREEN	to	Gscom coax socket
BLUE	to	Bcom coax socket

COMPOSITE input monitor (monochrome)

ORed planes (all colour planes have equal luminance) to "ORed" 3 plane video coax socket.
Grey scale to Vgrey coax socket.(many monitors have automatic gain control, in which case the red output will be very dim.

CHAPTER 5

MODIFYING RAM CARDS

NASCOM RAM TYPE "A"

Lift pin 1 of IC 35 and connect it to pin 10 of IC 35.
Lift pin 13 of IC 21 and connect it to pin 2 of IC 35 and connect this via a 10 K ohm resister to + 5 Volts.

NASCOM RAM TYPE "B"

This is the normal system ram card for NASCOM 2 and 3 microcomputers.

Remove LINK 5
And link together test pins WR EN and RD EN.

NOTE for RAMB cards using the page mode option the above modification will disable the normal page mode operation. The AVC pages out ram using the NAS-BUS signal /RAMDIS, however so as not to corrupt the ram data it asserts the /RAMDIS signal for both READ and WRITE. This means that the ram card must be modified so that /RAMDIS BOTH WRITE AND READ PROTECTS THE RAM.

IMPORTANT.

THIS REQUIREMENT THAT THE /RAMDIS SIGNAL BOTH WRITE AND READ PROTECTS THE SYSTEM RAM CARD (at the current program counter address) APPLIES TO ALL RAM, EPROM AND ROM IN THE SYSTEM.
IT SHOULD BE NOTED THAT ANY RAM, EPROM OR ROM ON THE MAIN PROCESSOR BOARD IS NOT AFFECTED BY /RAMDIS. THEREFORE A MODIFICATION MUST BE MADE IF THE AVC IS PAGED OVER THIS MEMORY.
SHOULD THE USER'S SYSTEM PRECLUDE THE USE OF RAMDIS THEN TEST PIN 17 ON THE AVC CAN BE USED.
Ram A boards should either not have EPROM located under the AVC paging area (8000H-BFFFH) or if it has to be then use /RAMDIS to disable the data bus buffers.

'64 K RAM CARD' *GEMINI*

Lift PIN 10 of IC 48 (74LS00) and connect this to PIN 4 of IC 22 (74LS20).
Note page mode operation will not be affected.
The page mode link should be set for page mode operation.

CHAPTER 6

INSTALLATION OF THE AVC

ON NASCOM 3 SYSTEMS (or Nascom 2)

[1] Modify the RAM B card as detailed in CHAPTER 5

[2] Connect the normal nascom video to the AVC's external video as detailed in chapter 4.

[3] Insert the AVC card into the card frame, the usual order is;

```
TOP  RAM B
     FLOPPY DISK CONTROLLER
     AVC
     PROCESSOR CARD
```

The suggested order is not critical.

[4] Remove the screened cable from the video output of the processor card and connect it to the compositive video output of the AVC. (see chapter 4)
Note either the GREY scale or the ORed coax socket.

REMEMBER THAT UNLESS NAS-SYS:AVC IS BEING USED THEN EVERY TIME AFTER POWER UP THE AVC SHOULD BE PAGED OUT. TO DO THIS TYPE

O B2 8Ø (under NAS-SYS, NAS-DOS)

NOTE THIS DOES NOT APPLY TO CP/M USER'S.

The AVC will work with NASCOM 1 systems directly if they are running at 4 MHz.

For any system running at 2 MHz then make the following modification to the AVC.

LINK 11 should be changed from C connected to 4 MHz to C connected to 2 MHz. (Remember to cut the standard default track)

[5] Many users will require to drive two displays, this can be achieved by connecting the first to the standard Nascom display and the second to the AVC.

[6] The AVC can drive a television set without the use of the PAL encoder (but using grey levels only).

1. Remove R71 and Tr 4 on the Nascom 2.
2. Connect either the grey or ored compositive output from the AVC to the emitter of Tr4 (junction of Tr4 e,R71,R22 and R76).
3. The television is connected as for a normal Nascom.

PROBLEMS:

[1] If any problems are encountered with bits flashing on the display then change the value of C13/C135 or C136.

[2] When connecting the output of the AVC to a colour monitor then use individually screened coax cables otherwise cross-talk may occur.

CHAPTER 7

DISCLAIMER

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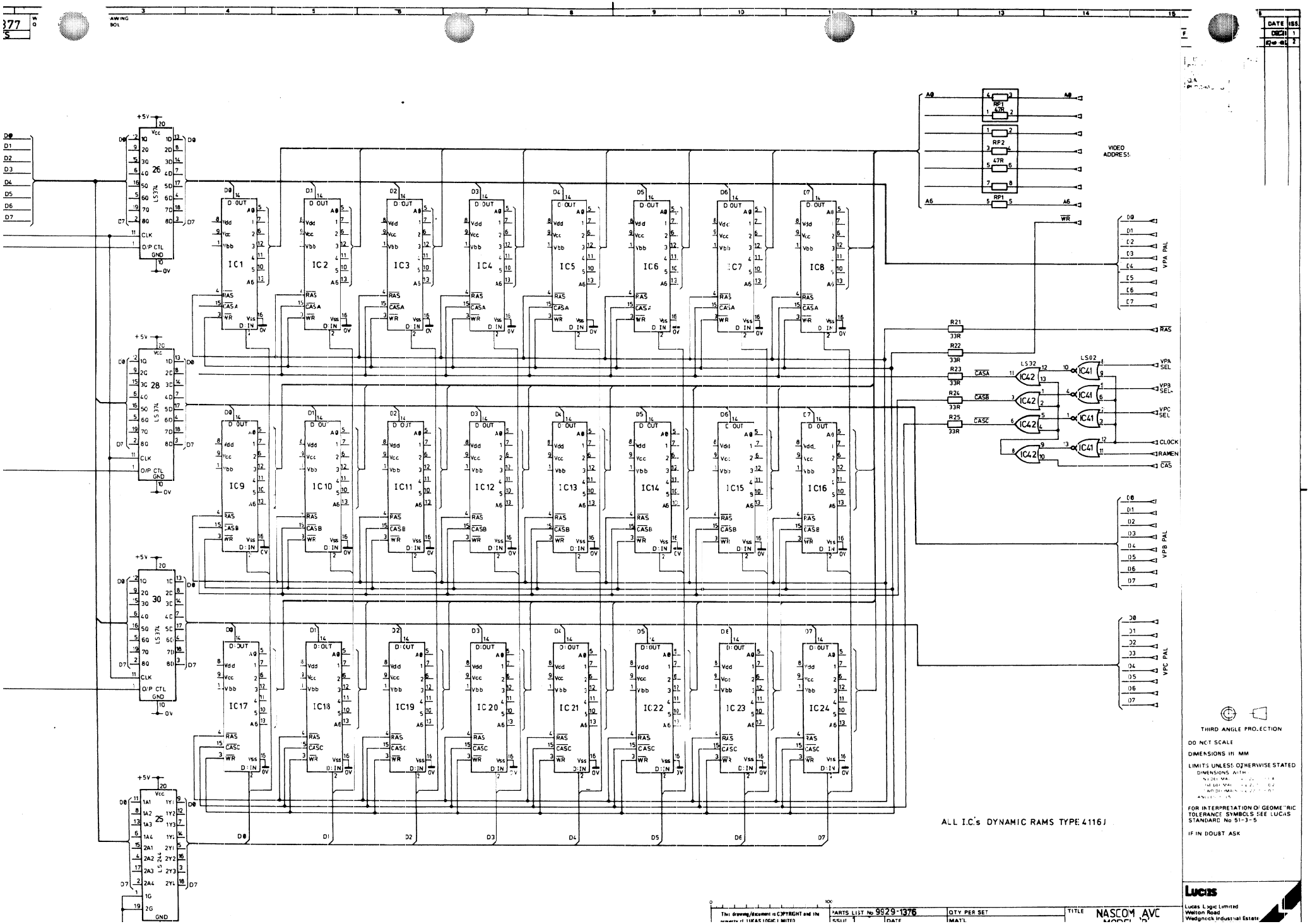
APPENDIX 1

AVC (MODEL B) CIRCUIT DIAGRAMS

Sheet 1 of 2 : MAIN CONTROL CIRCUITRY

Sheet 2 of 2 : VIDEO MEMORY PLANES



VIDEO ADDRESS
VPA PAL
VPB PAL
VPC PAL
RAS
VPA SEL
VPB SEL
VPC SEL
CLOCK
RAMEN
CAS
LS32
LS02
LS374
LS244
ALL I.C.'s DYNAMIC RAMS TYPE 4116J
THIRD ANGLE PROJECTION
DO NOT SCALE
DIMENSIONS IN MM
LIMITS UNLESS OTHERWISE STATED
FOR INTERPRETATION OF GEOMETRIC TOLERANCE SYMBOLS SEE LUCAS STANDARD No 51-3-5
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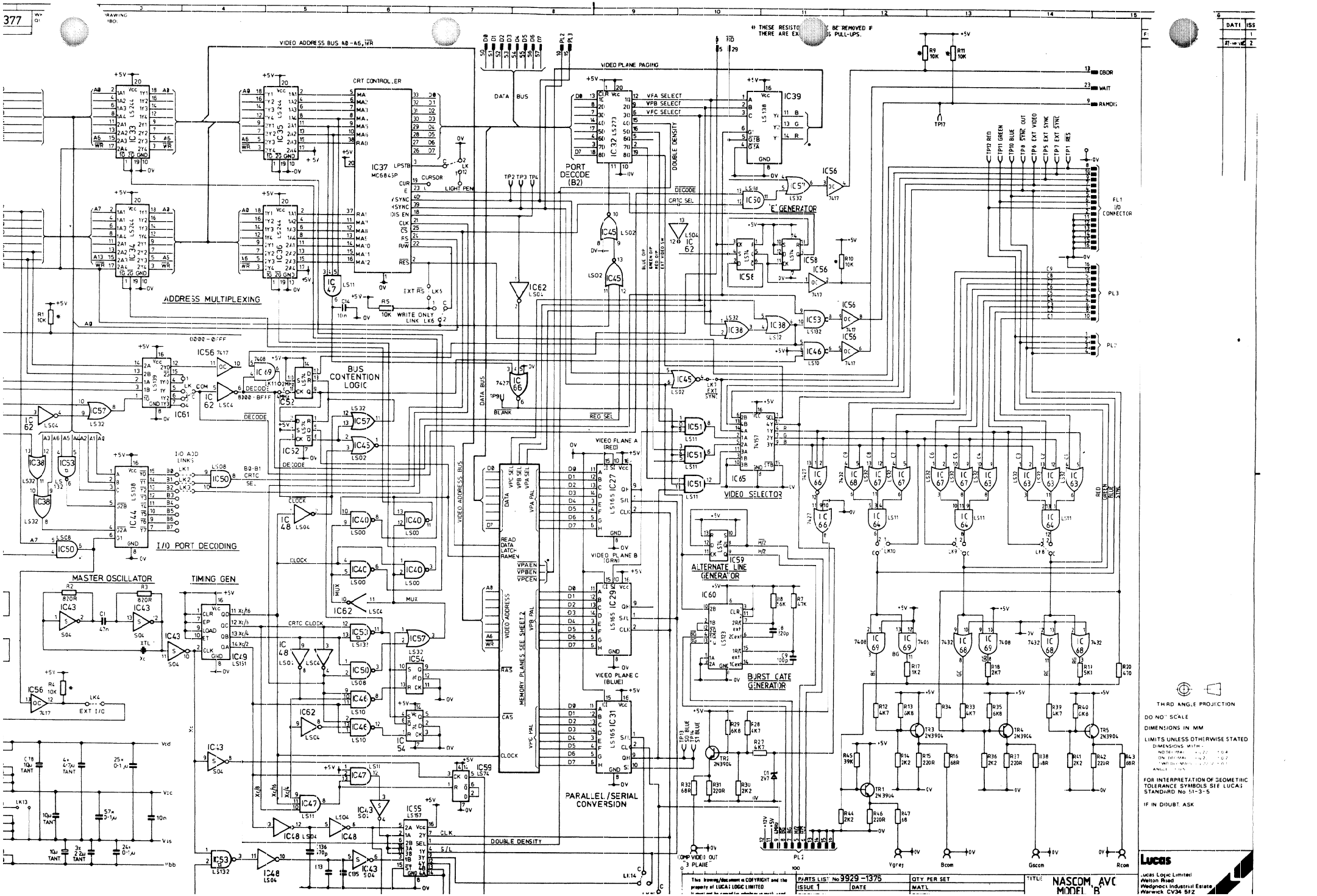
VIDEO ADDRESS BUS A0-A6, WR
DATA BUS
VIDEO PLANE PAGING
CRT CONTROLLER
IC37 LPSTB MC6845P
PORT DECODE (B2)
DOUBLE DENSITY
VFA SELECT
VFB SELECT
VFC SELECT
IC39
'E' GENERATOR
ADDRESS MULTIPLEXING
BUS CONTENTION LOGIC
I/O ADD LINKS
I/O PORT DECODING
MASTER OSCILLATOR
TIMING GEN
VIDEO PLANE A (RED)
VIDEO PLANE B (GRN)
VIDEO PLANE C (BLUE)
VIDEO SELECTOR
ALTERNATE LINE GENERATOR
BURST GATE GENERATOR
PARALLEL/SERIAL CONVERSION
MEMORY PLANES SEE SHEET 2
READ DATA LATCH RAMEN
DBOR
WAIT
RAMDIS
FL1 I/O CONNECTOR
PL3
PL4
PL5
TP17
TP12 RED
TP11 GREEN
TP10 BLUE
TP9 SYNC OUT
TP6 EXT VIDEO
TP5 EXT SYNC
TP7 EXT SYNC
TP1 RES
THIRD ANGLE PROJECTION
DO NOT SCALE
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