nascom

Nascom 2 Microcomputer
DOCUMENTATION

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ISSUE	DATE	REVISED SHEETS	REMARKS
1.	18.9.78.	(i) - (ii), 1-1,2-1, 3-1-3.3, 4-1, 5-1, A. 1-A.2, B.2-B.2, C. 1-C.2.	First formal issue
2.	11.1.79	(i)-(ii), 2.1,3.1-3.3, 4.1, 5.1, C.2.	Revision of detail.
3.	18.10.79	(i)-(ii), 1-5, App. A-C	Revised for compatibility with NASCOM 2.

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TITLE: NASBUS Functional Specification	

CONTENTS

1. Introduction

The NASBUS is a bus used to add extra boards (e.g. memory and I/O) to the basic NASCOM Microcomputer. It consists mainly of buffered Z80 input and output signals together with some additional bus control lines.

The equipment practice used has been chosen for its wide availability and low cost.

This document defines the electrical and physical characteristics of the NASBUS.

2. References

This specification should be read in conjunction with the following documents:

1. Z80 Microcomputer devices Technical Manual MK 3880 Central Processing Unit - Mostek.
2. VERO catalogue.
3. Mostek Z80 Technical Manual
   MK 3881 Parallel I/O Controller

3. Functional Description

The Nasbus is a 77 way bus, with signals allocated as described below. Please see the Z80 CPU manual (1) for details of timing and operation of Z80 derived signals.

Note that lines marked "Reserved" have already been allocated for future use.

PIN	SIGNAL NAME	DESCRIPTION
1	Ov	
2	Ov	
3	Ov	Power supply and system ground
4	Ov	
5	Clock	Buffered system clock 1/2 MHz for Nascom 1. 2/4 MHz for Nascom 2.
6	$\overline{\text{NMI SWITCH}}$ *	An active low signal which initiates a short pulse on the Z80 CPU $\overline{\text{NMI}}$ pin (but not necessarily on bus line 21). Nascom 2 provides this facility.
7	(reserved)	
8	(reserved)	
9	$\overline{\text{RAM DISABLE}}$*	An active low signal which disables output from any RAM on the bus. Used to give ROM priority over RAM.
10	$\overline{\text{RESET SWITCH}}$ *	An active low signal which initiates a short pulse on the $\overline{\text{RESET}}$ line (pin 14), to reset the system without destroying dynamic RAM contents.
11	$\overline{\text{NASCOM MEM}}$	A decoded signal from one of the RAM boards in the system defining which 4K memory block is used by the NASCOM 1. (Usually OOOOH - OFFFH). Not used by NASCOM 2.
12	$\overline{\text{NASCOM IO}}$	A decoded signal from an IO expansion card defining which ports are used on the NASCOM.
13	$\overline{\text{DBDR}}$ *	This signal 'Data bus drive' determines the direction of the bidirectional data bus buffers on the NASCOM Buffer card. It is a decoded signal made active by any device transferring data to the NASCOM card. Active low to drive data to the NASCOM. (Although this signal is not used by NASCOM 2 it must be generated by any peripheral card to ensure operation with a buffered NASCOM 1).
14	$\overline{\text{RESET}}$ *	The main system reset line. The duration of of the RESET pulse is restricted to about 7 uS. to maintain dynamic RAM refresh. The line is unbuffered and bidirectional, i.e. the $\overline{\text{RESET}}$ signal may be either generated or used by any card in the bus.
15	$\overline{\text{HALT}}$	Buffered Z80 $\overline{\text{HALT}}$ signal.
16	$\overline{\text{BAI}}$ * * or $\overline{\text{TEST}}$ *	These signals are used to provide a 'daisy chain' Bus acknowledge signal for priority bus control during DMA. On the NASCOM 2 CPU card line 16 (normally $\overline{\text{BAI}}$) is used for an active low $\overline{\text{TEST}}$ facility which floats the address and most control signal buffers. As usual for a CPU card, line 17($\overline{\text{BAO}}$) = buffered CPU $\overline{\text{BUSAK}}$ signal.
17	$\overline{\text{BAO}}$ * *	
18	$\overline{\text{BUSRQ}}$ *	Z80 $\overline{\text{BUSRQ}}$ signal. Used by external devices to request control of the data, address and control lines.
19	IEI * *	These signals form a 'daisy chain' connection for interrupt priority control.
20	IEO * *	
21	$\overline{\text{NMI}}$ *	On the NASCOM 1 the Z80 Non Maskable Interrupt is dedicated to the monitor single step feature. This line is reserved for $\overline{\text{NMI}}$ for users who require to generate this signal on the bus and is accepted as a buffered input by the NASCOM 2.
22	$\overline{\text{INT}}$ *	Z80 interrupt request line.
23	$\overline{\text{WAIT}}$ *	Z80 $\overline{\text{WAIT}}$ line

PIN	SIGNAL NAME	DESCRIPTION
24	$\overline{\text{RFSH}}$	Tristate buffered Z80 $\overline{\text{RFSH}}$ signal
25	$\overline{\text{MI}}$	Tristate buffered Z80 $\overline{\text{MI}}$
26	$\overline{\text{IORQ}}$	Tristate buffered Z80 $\overline{\text{IORQ}}$
27	$\overline{\text{MREQ}}$	Tristate buffered Z80 $\overline{\text{MREQ}}$
28	$\overline{\text{WR}}$	Tristate buffered Z80 $\overline{\text{WR}}$
29	$\overline{\text{RD}}$	Tristate buffered Z80 $\overline{\text{RD}}$
30	A0	
31	A1	
32	A2	
33	A3	
34	A4	
35	A5	
36	A6	
37	A7	
38	A8	Tristate Z80 Address lines 0 to 15
39	A9	
40	A10	
41	A11	
42	A12	
43	A13	
44	A14	
45	A15	
46	)	
47	) Reserved	
48	)	
49	)	
50	D0	
51	D1	
52	D2	
53	D3	
54	D4	Bidirectional, Tristate Z80 Data lines
55	D5	0 to 7.
56	D6	
57	D7	
58	)	
59	)	
60	)	
61	) Reserved	
62	)	
63	)	
64	)	
65	)	
66	Unused (to provide separation of signal and power lines).	
67		
68	-5V	Power supply
69	-5V	" "
70	-12V	" "
71	-12V	" "
72	Keyway	
73	+12V	Power supply
74	+12V	" "
75	+ 5V	" "
76	+ 5V	" "
77	+ 5V	" "
78	+ 5V	" "

* = "Open Collector" signal line

** note (i) link on any card not using these (IEI - IEO and/or $\overline{\text{BAI}}$ - $\overline{\text{BAO}}$).
(ii) bus tracks must be broken near any card socket using these lines
(iii) buffer card and NASCOM 2 provide a pull up resistor for IEO

Designers should recognise that the frequency of the system clock may change at some future date (as a result of system upgrades/improvements) and should allow for this possibility.

4. Electrical Specification

4.1 Tristate Logic

These lines are driven by low power Schottky tristate buffers capable of sinking 16 mA-i.e. capable of driving 10 standard TTL loads (1.6mA sinking, 40 u A source) or approximately 40 low power Schottky inputs (0.36 mA sinking, 20 u A source) while retaining logic zero $\leq$0.4v and logic 1$\geq$2.4v.

4.2 Open Collector

Open collector lines are pulled up to 5 v. Any board can pull down to zero provided it is capable of sinking 16 mA.

4.3 Power supplies

In order to avoid overloading the motherboard and the system power supplies the following rules should be applied.

(a) All bus lines of the same voltage should be commoned on any plug-in board.

(b) No board should draw a total of more than:

+	5v	2.0 Amps
-	5v	0.5 Amp
+	12v	1.0 Amp
-	12v	0.5 Amp

(c) The whole occupied Nasbus should not draw more than:

+	5v	8 Amps
-	5v	1 Amp
+	12v	2 Amps
-	12v	1 Amp

4.4 General Design Points

Boards should be designed where possible to apply no more than 2 or 3 low power loads to any signal line of the Nasbus. In any event, a maximum of 1 TTL load must not be exceeded.

Capacitance limits of 40pF for Data bus lines and 20pF for all others are advised.

The above figures may be somewhat exceeded on a CPU card.

$\overline{RD}$, $\overline{WR}$, $\overline{MREQ}$, $\overline{IORQ}$, $\overline{MI}$, $\overline{RFSH}$ should be pulled up to +5v with a 10K resistor where feasible.
Note that tristate lines will float if the Nascom CPU is disabled e.g. by a bus request.

No board may be plugged into or removed from the bus when power supplies are live. It is advisable to wait for up to 2 minutes after switching supplies "off".

5. Physical Specification

5.1 Board Specification

5.1.1 Board Dimensions

The standard board size is 203.20mm long + 0.00, - 0.30 by 203.20mm. high + 0.00, - 0.25 (i.e. 8 x 8 inches). The thickness should be 1.60 nominal (including copper). See also Appendix A.

A suitable prototyping board is Vero type 10-0155 F (up to 45 DIPs) Type Nos. 06-3462C and 06-3463J can also be used.

5.1.2 Contact Pitch

The contact pitch is 2.54mm. 77 of the possible 78 ways are used, with a reference key 7 from the bottom. The contacts used are on the solder side, and it is recommended that they are hard gold plated.

5.2 Connector Specification

Suitable connectors are Vero type 14-0998G (with polarising key in position 72) or Varelco type 00.6072-080-657-101 with polarising key at position 73, positions 1 and 80 blank. (See Appendix B).

5.3 Mother Board Specification

Board Material

The preferred material is G10 or FR4 epoxy glass (because of the mechanical strains involved). However, a section of SRBP 78 way Veroboard type 67-1902F (about 15½" x 8") may be used with care.

5.3.2 Linking

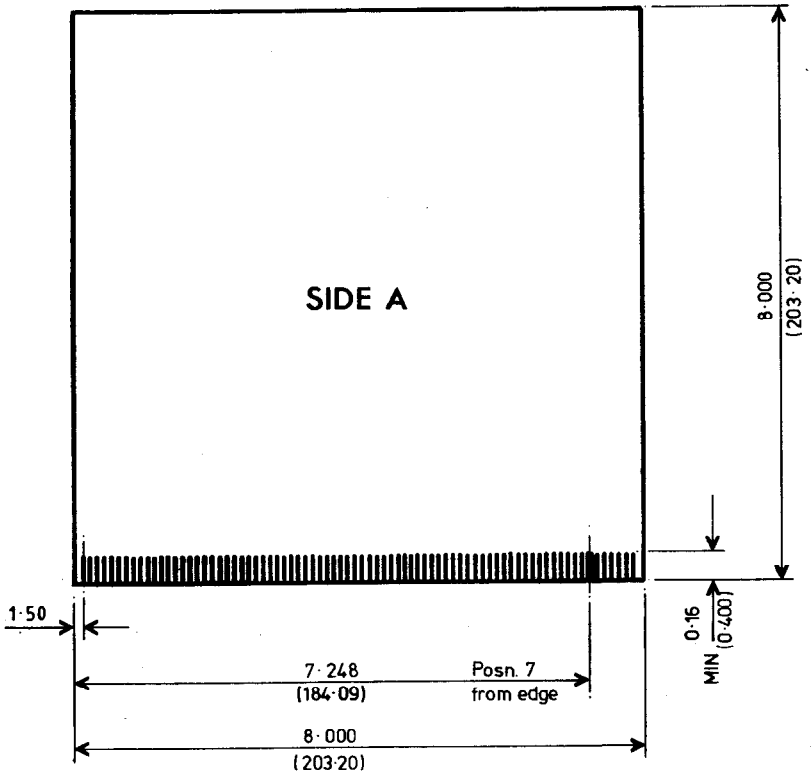
Appropriate power supply lines should be commoned together by links on the Mother Board.

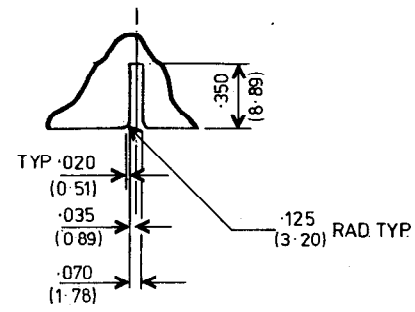
To reduce both AC Impedance and DC resistance of the two main supply rails it is advisable to add one length of, say, 22 SWG tinned copper wire behind the top 4 lines (Nos. 1-4 : 0V.) and another behind the bottom 4 lines (Nos.75-78 : +5v). These wires are easily fitted if the relevant 4 pins of each connector are bent together and the horizontal bus wires wound round them before soldering.

Lines 16 and 17, and 19 and 20 should be cut and linked between sockets to provide daisy chain Bus Acknowledge and Interrupt Enable signals (see section 3 and reference 3).

APPENDIX A

BOARD OUTLINE

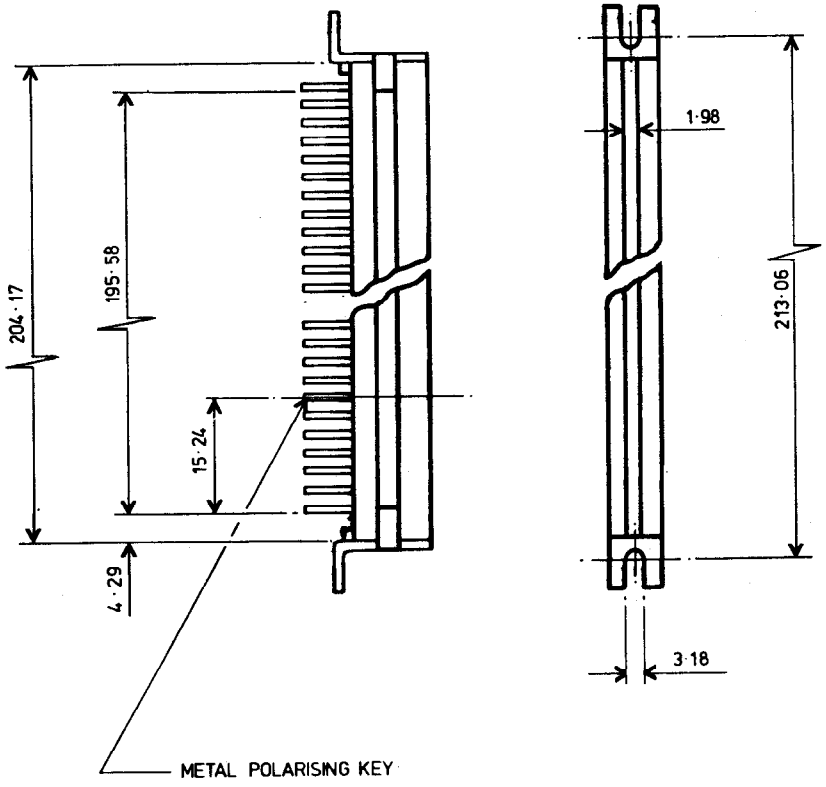




Detail of Polarising Key

APPENDIX B

CONNECTOR OUTLINE



APPENDIX C

NASBUS SUMMARY

Lines marked * are open collector: those overlined are $\overline{\text{NOT}}$ (logic level).

1,2,3,4	0V: GROUND
5	Ø (buffered clock)
6	$\overline{\text{NMI}}$ SWITCH *
7,8	reserved
9	$\overline{\text{RAMDISABLE}}$*
10	$\overline{\text{RESET}}$ SWITCH *
11	$\overline{\text{NASCOM MEM}}$
12	$\overline{\text{NASCOM IO}}$
13	$\overline{\text{DBDR}}$*
14	$\overline{\text{RESET}}$*
15	$\overline{\text{HALT}}$
16	$\overline{\text{BAI}}$ (or $\overline{\text{TEST}}$* for CPU card)
17	$\overline{\text{BAO}}$
18	$\overline{\text{BUSRQ}}$*
19	IEI
20	$\overline{\text{IEO}}$
21	$\overline{\text{NMI}}$*
22	$\overline{\text{INT}}$*
23	$\overline{\text{WAIT}}$*
24	$\overline{\text{RFSH}}$
25	$\overline{\text{M1}}$
26	$\overline{\text{IORQ}}$
27	$\overline{\text{MREQ}}$
28	$\overline{\text{WR}}$
29	$\overline{\text{RD}}$
30	A0
31	A1
32	A2
33	A3
34	A4
35	A5
36	A6
37	A7
38	A8
39	A9
40	A10
41	A11
42	A12
43	A13
44	A14
45	A15
46, 47, 48, 49	Reserved
50	D0
51	D1
52	D2
53	D3
54	D4
55	D5
56	D6
57	D7
58, 59, 60 ... 65	Reserved
66, 67	To separate signal and power lines
68, 69	-ve 5V
70, 71	-ve 12V
72	KEY
73, 74	+ve 12V
75, 76, 77, 78	+ve 5V

INTERRUPT AND BUS ACKNOWLEDGE DAISY CHAINS

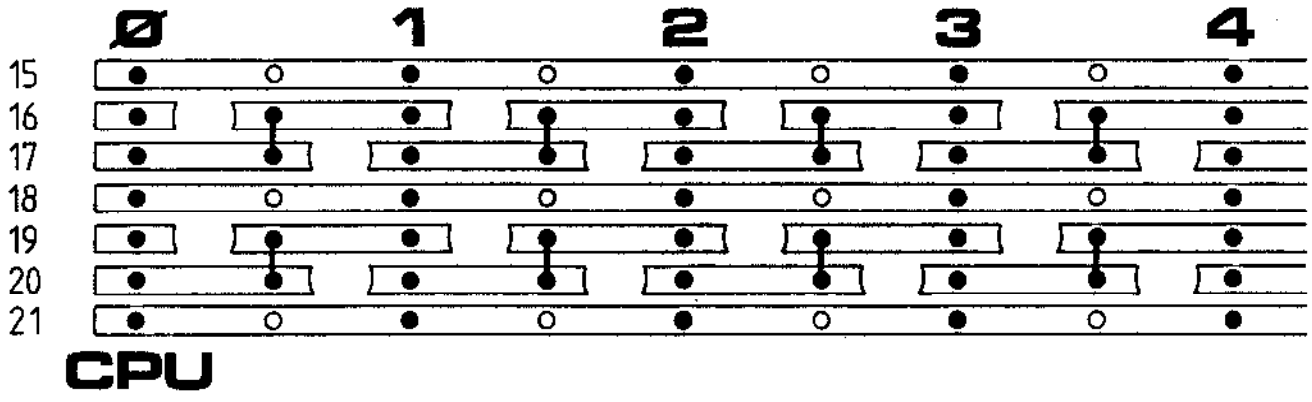
It is necessary to assign to each board in the system a priority for use of the bus and for operation of interrupts. It is conventional to assign the same priority for each function to a given board.

Lines 16 and 17 of NASBUS provide the bus acknowledge daisy chain lines; lines 19 and 20 are used for the interrupt enable daisy chain. It is necessary for one signal of each pair to enter boards always on the same bus line, the other leaving boards on the adjacent line. Inputs ($\overline{BAI}$ and IEI) are on lines 16 and 19 respectively, outputs ($\overline{BAO}$ and IEO) being adjacent on lines 17 and 20 respectively. Clearly the use of a normal motherboard will frustrate operation of these systems, since all inputs will be common, as will the outputs. Modification of the motherboard will therefore be required in large systems to ensure correct operation of the priority systems and to permit priority selection of the boards in the computer system.

Veroboard motherboards should be modified exactly in accordance with the diagram below. NASCOM MaxiMotherboards should be wired according to the instructions supplied with them; it should be noted that they may be set up to assign priority from either end of the bus. NASCOM MiniMotherboards are already wired for priority and assign it automatically.

Care should be taken in the construction of unusual systems, particularly those in which the bus is driven unconventionally, to ensure that line 16 is always driven by line 17 and that line 19 is always driven by line 20.

In the conventional arrangement the board furthest from the CPU board's point of access to the bus is assigned the highest priority; this does not imply that the motherboard slot at the far end of the bus need necessarily be used; it is desirable to expand the bus from the processor end, moving all boards along as necessary to preserve the priority structure. This technique will reduce the propagation effects of an extended bus as far as is possible.



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NASCOM FRAME KIT

Parts List

Qty	Item
1	Left Side Panel
1	Right Side Panel
1	Backplane board
8	Card guides
4	M3 screws
4	M3 star washers
4	M3 nuts
4	No 6 self tapping screws
5	Terminal pins

Instructions (refer to drawing)

1) Solder the terminal pins to the 5 power supply points on the backplane board

2) Solder the 77 way edge connectors from your Nascom Kits to the backplane - mounting them with the contacts towards the bottom of the board.

3) Solder a sleeved wire link from SK2 pin B71 to SK3 pin B71 (-12v rail).

4) Solder a sleeved wire link from SK2 pin B73 to SK3 pin B73 (+12v rail).

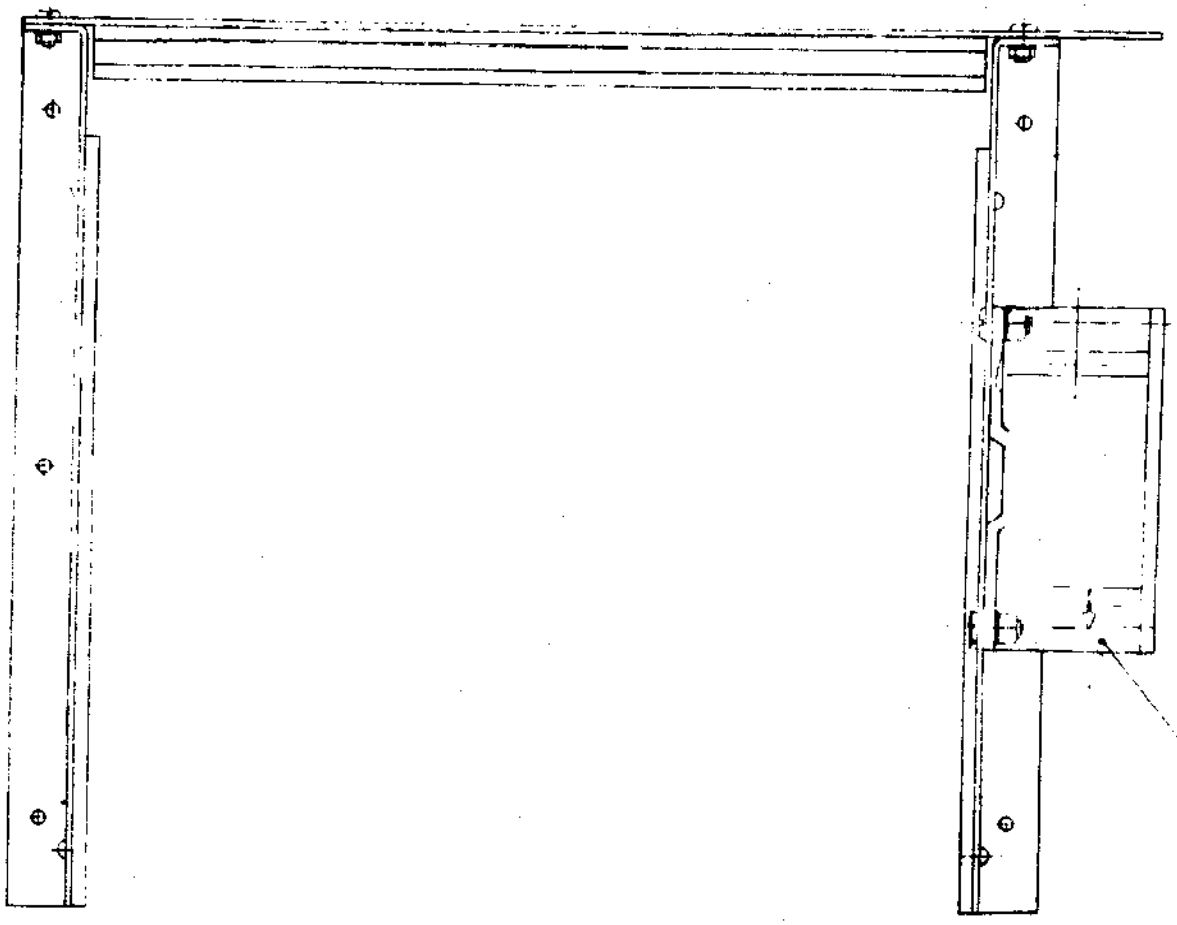
5) Solder a sleeved wire link from SK2 pin B76 to SK3 pin B76 (+5v rail).

6) Fit the card guides to each side panel.

7) It is recommended that a fan is fitted on the left side panel if more than one Nascom board is to be used in the Nascom case.

8) Assemble the side panel to the backplane with the screws, star washers and nuts provided.

9) Self tapping screws are provided to mount the Nascom frame in the Nascom case.


FAN
THIS IS NOT
SUPPLIED WIT-
THE KIT